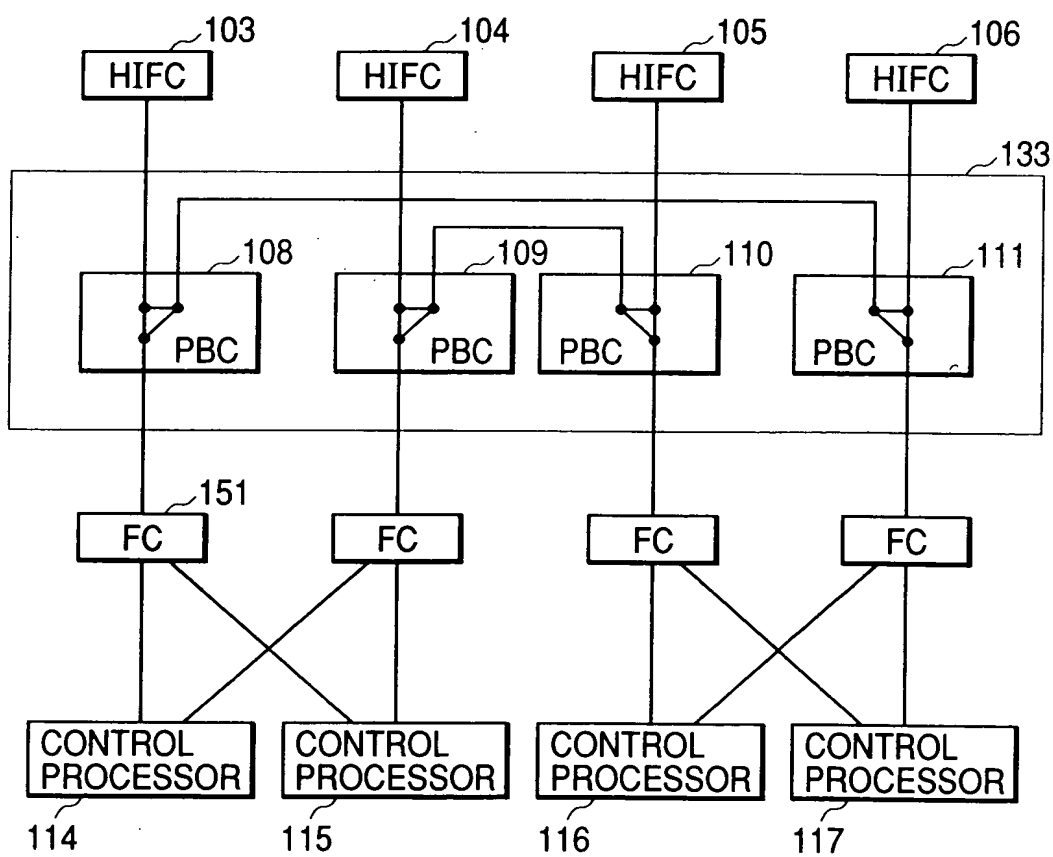


The diagram illustrates a storage system architecture. At the top, three **HOST COMPUTER** units (100, 101, 102) are connected to a central **LOOP** (133) via **HIFC** (Host Interface Function Controller) units (103, 104, 105, 106). Below the **LOOP**, there are four **CONTROL PROCESSOR** units (114, 115, 116, 117) and two additional **CONTROL PROCESSOR** units (119, 120) located within the **DISK CONTROLLER** section. The **CONTROL PROCESSOR** units (114, 115, 116, 117) are connected to the **LOOP** and a **SHARED CONTROL MEMORY** (112) containing **FCAL MANAGEMENT INFORMATION** (113). The **CONTROL PROCESSOR** units (119, 120) are connected to **DIFC** (Data Interface Function Controller) units (123, 124). The **DIFC** units (123, 124) are connected to a stack of four disk drives (127, 128, 129, 130) via **125** and **126**. A **SERVICE PROCESSOR** (131) is connected to the **DISK CONTROLLER** section. A **CACHE MEMORY** (122) is also connected to the **DISK CONTROLLER** section. The **DISK CONTROLLER** section is labeled 107.

FIG. 2



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[illegible]

113	201	202	203
CONTROL PROCESSOR NUMBER	AL-PA	LUN	
114	EF	0—9	
115	E8	10—19	
116	E4	20—29	
117	E2	30—39	

```
graph TD; START([START]) --> 301[READ AL-PA ON A FRAME]; 301 --> 302{DOES THE AL-PA COINCIDE WITH THE PROCESSOR'S AL-PA?}; 302 -- NO --> 305[EXECUTE THE I/O REQUEST]; 302 -- YES --> 303[READ THE FRAME]; 303 --> 304[CHECK THE LUN ON THE FRAME]; 304 --> 305; 305 --> END([END]);
```

The flowchart illustrates the process of determining if the AL-PA coincides with the processor's AL-PA. It begins with a START terminal, followed by step 301: READ AL-PA ON A FRAME. Step 302 is a decision diamond: DOES THE AL-PA COINCIDE WITH THE PROCESSOR'S AL-PA?. If the answer is NO, the process proceeds to step 305: EXECUTE THE I/O REQUEST. If the answer is YES, the process proceeds to step 303: READ THE FRAME, then step 304: CHECK THE LUN ON THE FRAME, and finally to step 305. All paths converge at step 305, which then leads to the END terminal.

**FIG. 5**

FCAL MANAGEMENT INFORMATION		
113 CONTROL PROCESSOR NUMBER	201 AL-PA	202 LUN
114	EF	0—9
114	E8	10—19
115	—	—
116	E4	20—29
117	E2	30—39

**FIG. 6**

FCAL MANAGEMENT INFORMATION		
113	201	202
CONTROL PROCESSOR NUMBER	AL-PA	LUN
114	EF	0—9
115	—	—
116	E8	10—19
116	E4	20—29
117	E2	30—39

**FIG. 7**

FCAL MANAGEMENT INFORMATION		
113 CONTROL PROCESSOR NUMBER	201 AL-PA	202 LUN
114	EF	0—9
115	E8	10—14
116	E4	15—29
117	E2	30—39

FIG. 8

